**BIRLA INSTITUTE OF SCIENCE AND TECHNOLOGY PILANI, HYDERABAD CAMPUS**

**DIGITAL DESIGN LABORATORY (Session 2021-22)**

**Workbook**

**Experiment -5**

**Full Name of the Student: Shyam N V**

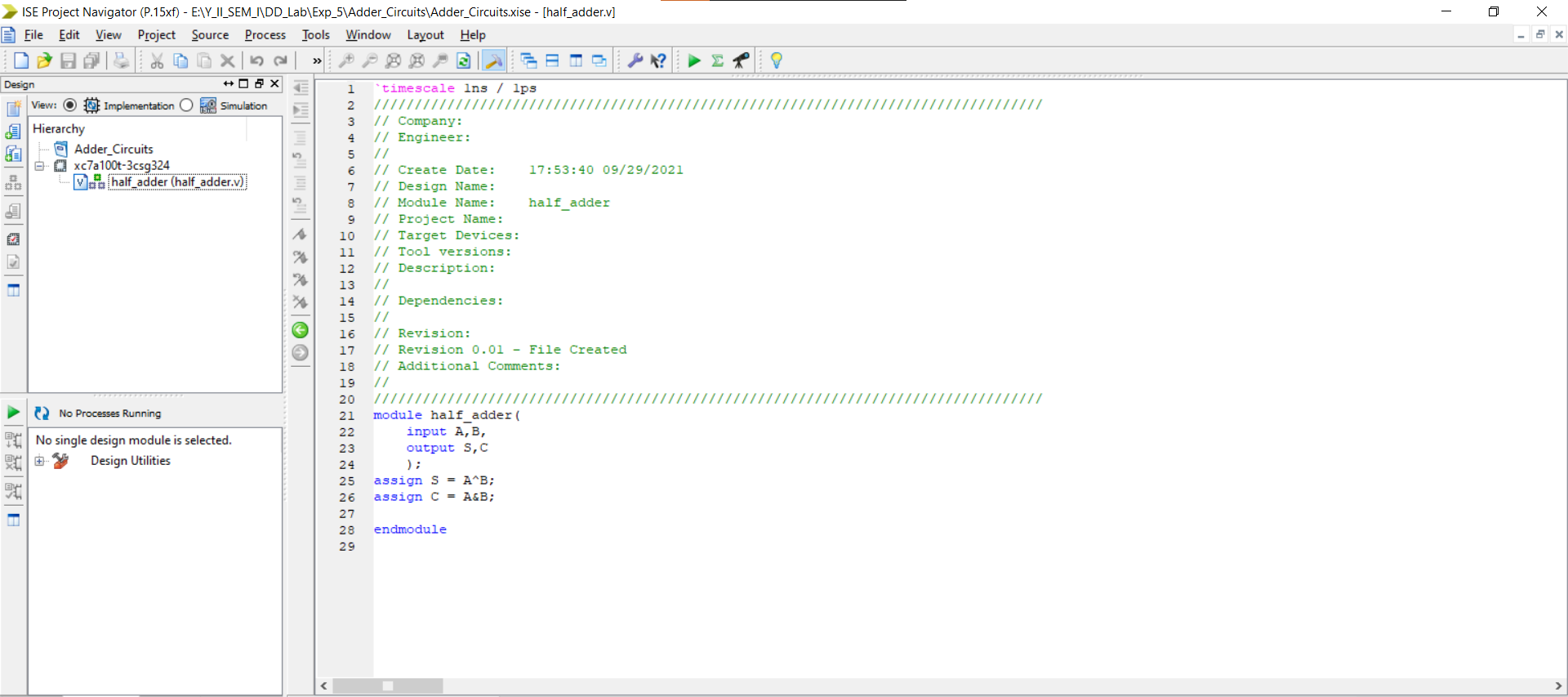
**Complete ID of the student: 2020A7PS2081H**

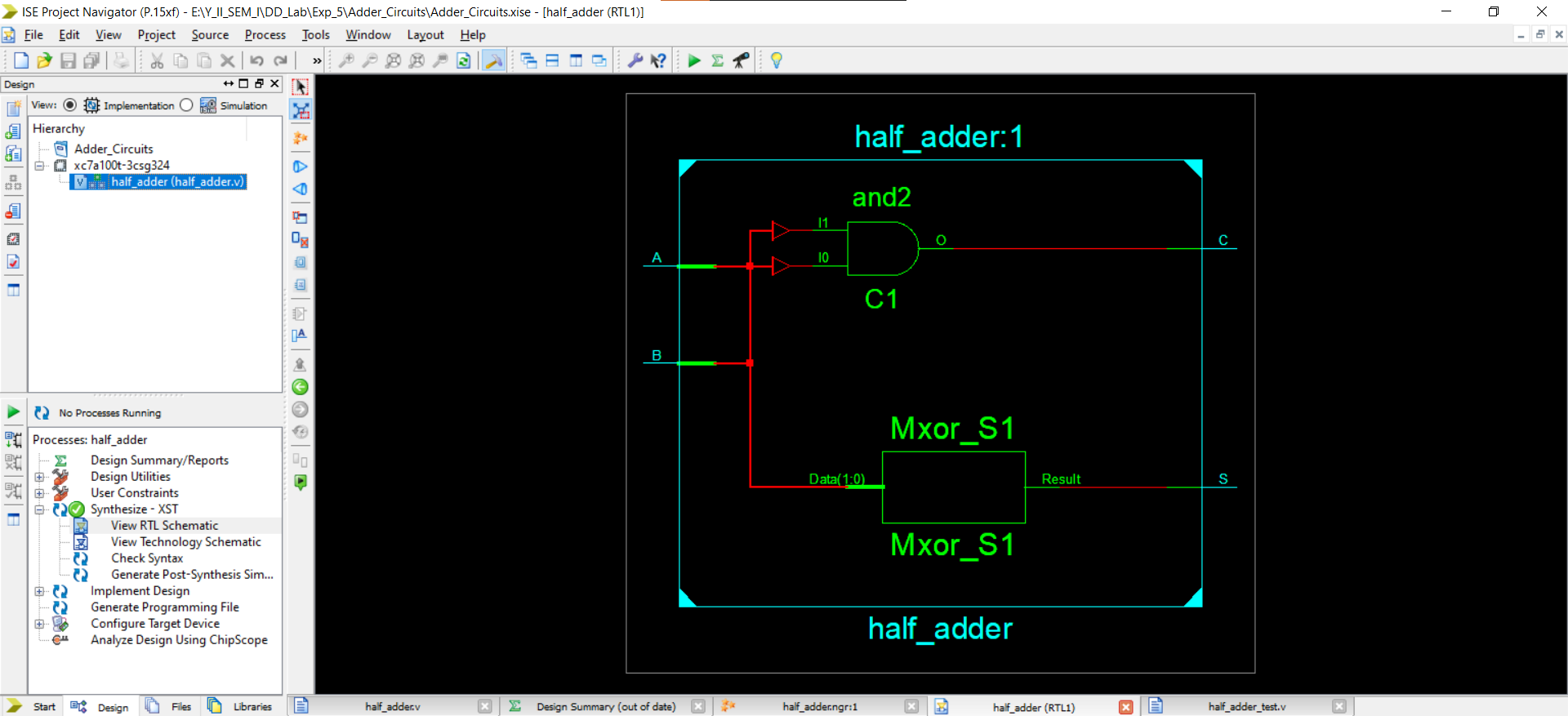
**Title of Experiment: Dataflow Modelling and Implementation of Adders**

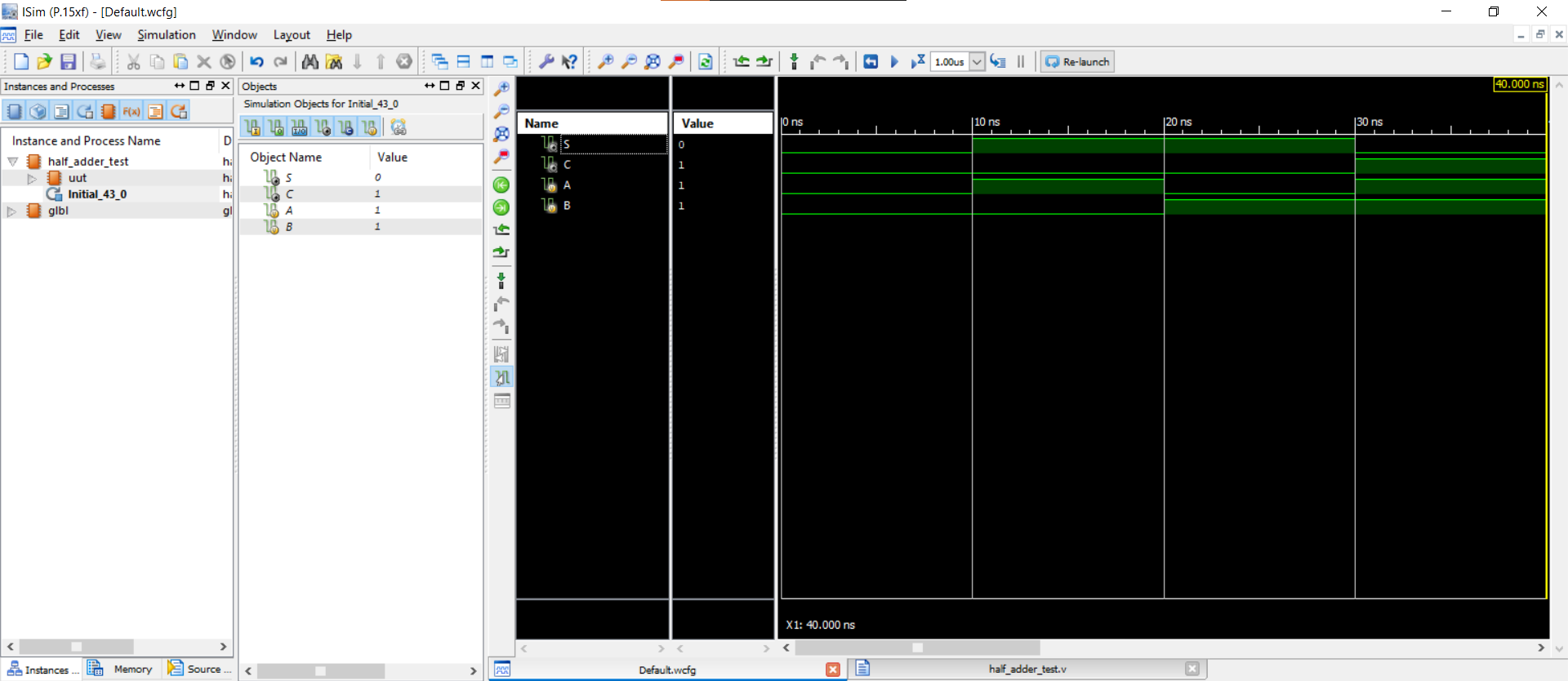
**Problem 1:**

**Implement the Half Adder circuit using Xilinx ISE**

**(Provide proper snapshots and Show the graphical output)**

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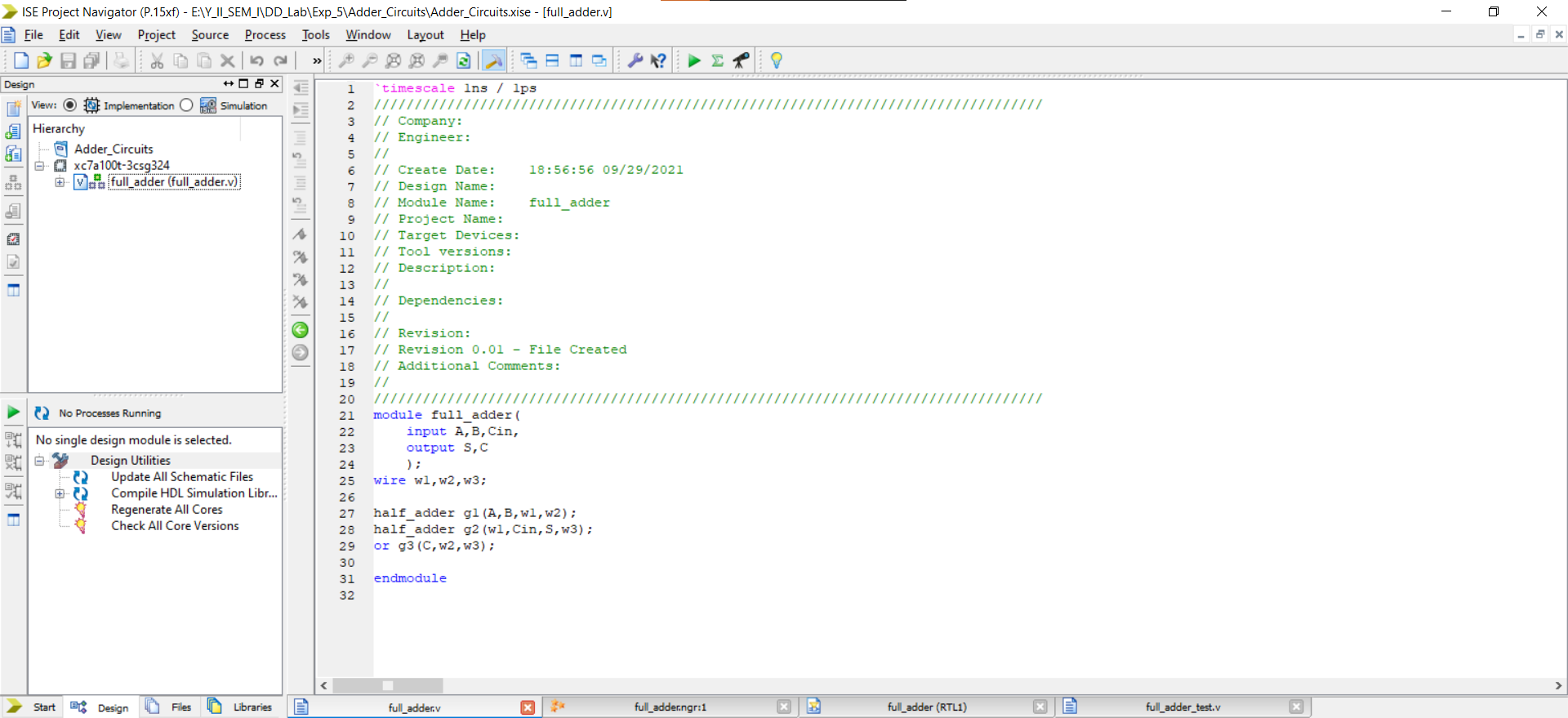
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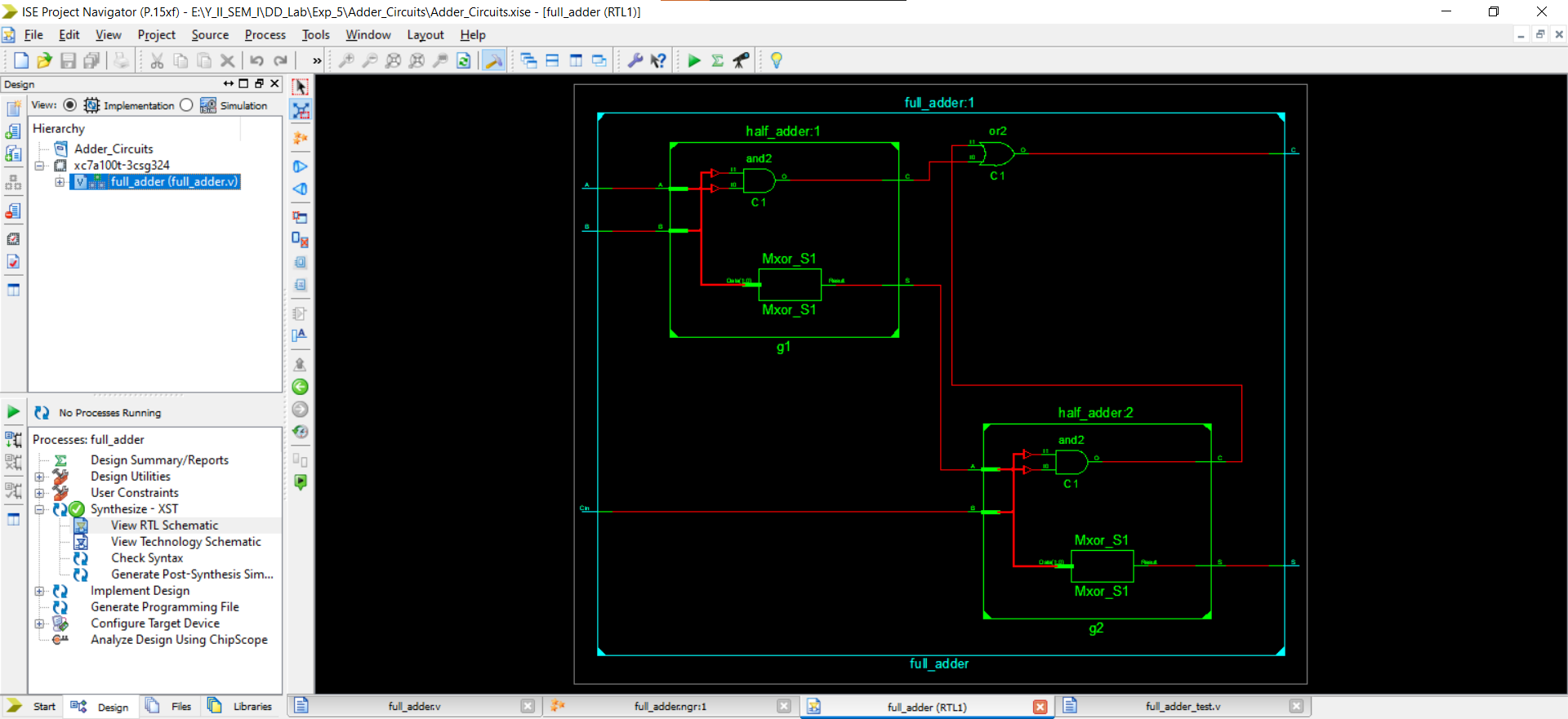
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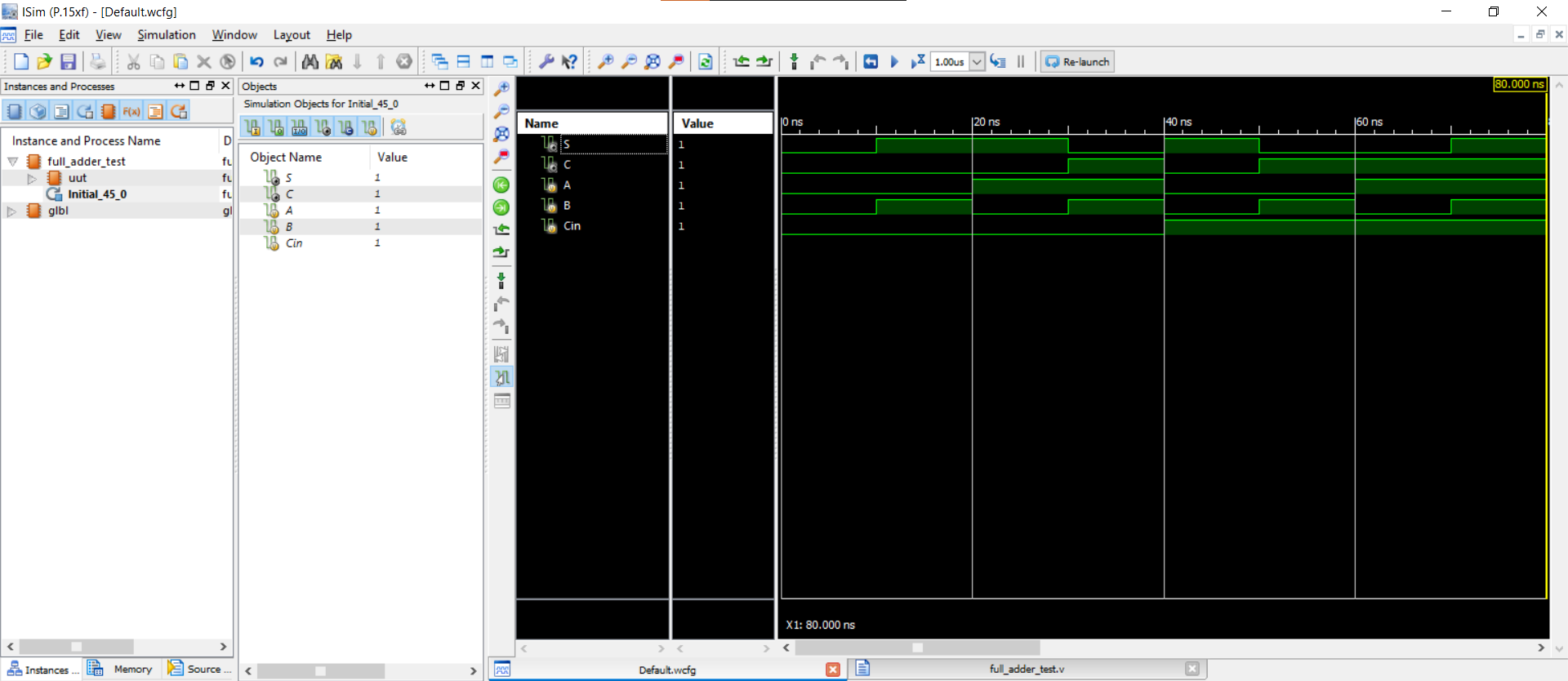
**Problem 2:**

**Implement Full Adder using Half Adders in Xilinx ISE**

**(Provide proper snapshots and show the graphical output)**

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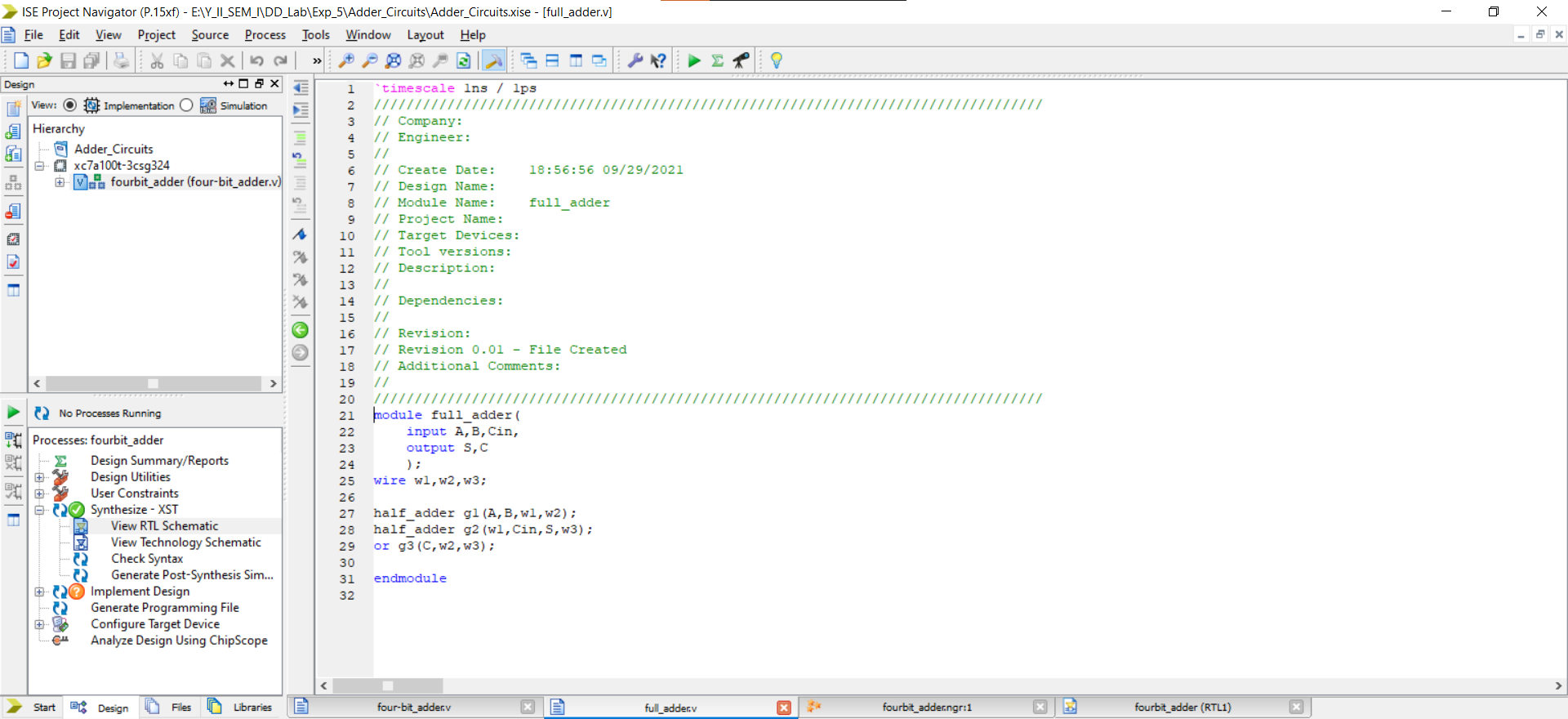
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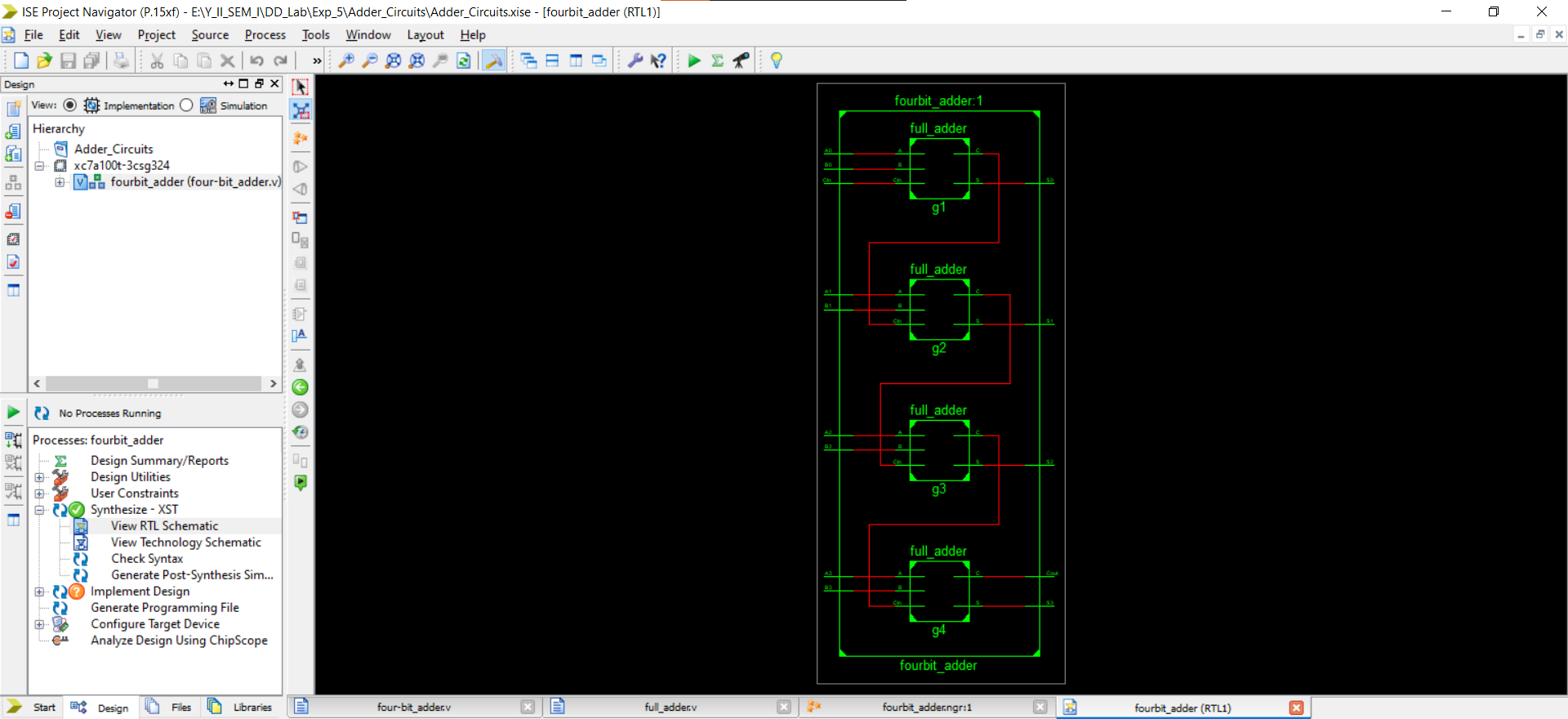
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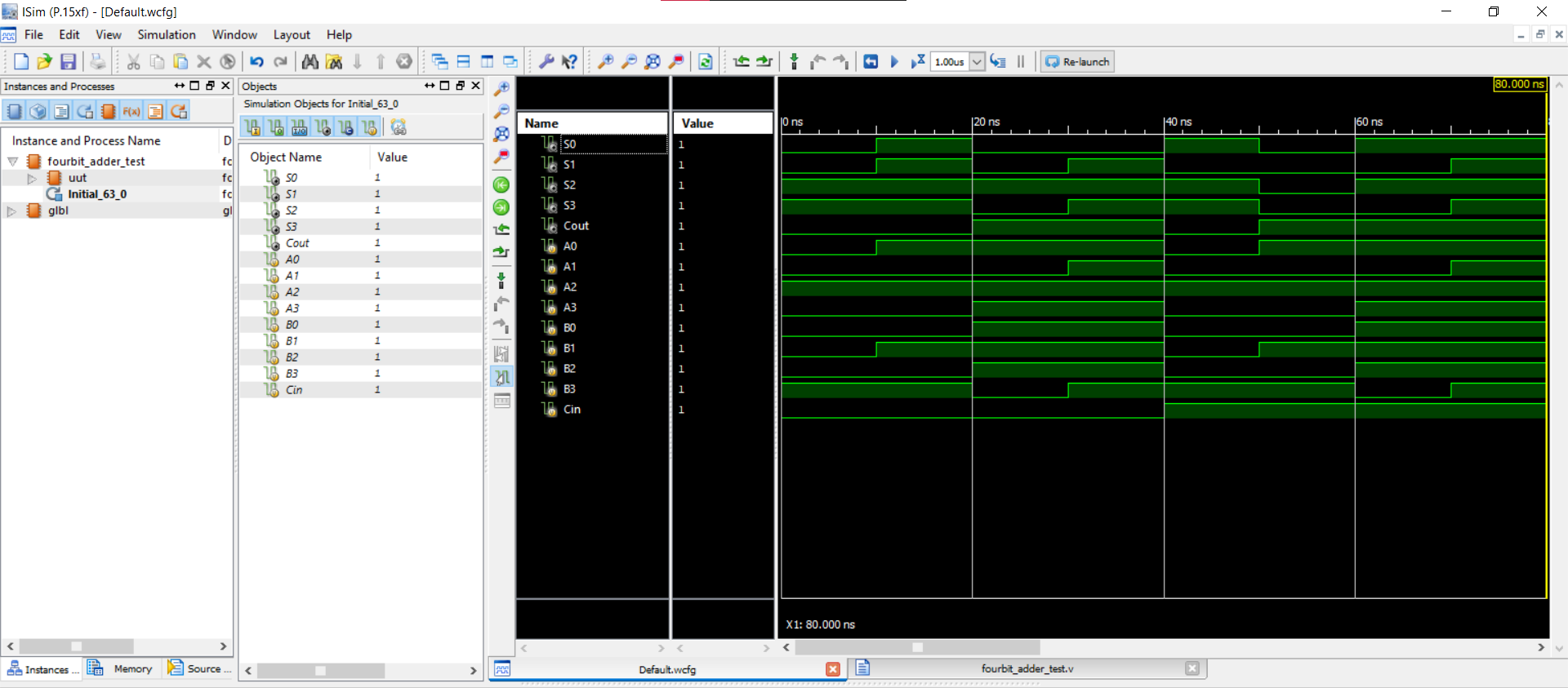
**Problem 3:**

**Implement 4-bit Full Adder in Xilinx ISE**

**(Provide proper snapshots and show the graphical output)**

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